IN THE CLAIMS

Please cancel claims 1-18 after adding the following new claims:

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19. A method of testing an integrated circuit by adjusting a semiconductor substrate bias voltage, the method comprising the steps of:

coupling the semiconductor substrate to a positive voltage supply through a series of resistive elements such that a voltage drop through the resistive elements defines a semiconductor substrate bias voltage having a first negative voltage level;

reducing the semiconductor substrate bias voltage to a second negative voltage level which is lower than the first negative voltage level by increasing the voltage drop through the resistive elements; and

increasing the semiconductor substrate bias voltage to a third negative voltage level which is higher than the first negative voltage level by decreasing the voltage drop through the resistive elements.

20. The method of claim 19 wherein the series of resistive elements are diodes.

21. The method of claim 20 wherein the step of reducing the semiconductor substrate bias comprises the step of electrically adding at least one additional diode to the series of diodes by deactivating a bypass transistor.

22. The method of claim 20 wherein the step of increasing the semiconductor substrate bias comprises the step of electrically removing at least one additional diode from the series of diodes by activating a bypass transistor.

23. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the

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substrate; and

coupling at least one bypass transistor to at least one diode in the series of diodes for electrically bypassing at least one diode.

24. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

25. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one bypass transistor to plurality of diodes for electrically bypassing the plurality of diodes.

26. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally off bypass transistor to at least one diode leaving the at least one diode unbypassed during normal operation and allowing the at least one diode to be selectively bypassed during testing operations.

27. (New) The method of claim 23 wherein coupling at least one bypass transistor to at least one diode includes coupling at least one normally on bypass transistor to at least one diode leaving the at least one diode bypassed during normal operation and allowing the at least one diode to be selectively unbypassed during testing operations.

28. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

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29. (New) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally off bypass transistor to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

30. (New) The method of claim 28 wherein coupling at least one bypass transistor to a plurality of diodes includes coupling at least one normally on bypass transistor to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

31 (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diodes between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

32. (New) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally off bypass transistors to a plurality of diodes leaving the plurality of diodes unbypassed during normal operation and allowing the plurality of diodes to be selectively bypassed during testing operations.

33. (New) The method of claim 31 wherein coupling a plurality of bypass transistors to a plurality of diodes includes coupling a plurality of normally on bypass transistors to a plurality of diodes leaving the plurality of diodes bypassed during normal operation and allowing the plurality of diodes to be selectively unbypassed during testing operations.

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34. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor.

35. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one bypass transistor to plurality of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

36. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally off bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor unbypassed during normal operation and allowing the at least one diode connected transistor to be selectively bypassed during testing operations.

37. (New) The method of claim 34 wherein coupling at least one bypass transistor to at least one diode connected transistor includes coupling at least one normally on bypass transistor to at least one diode connected transistor leaving the at least one diode connected transistor bypassed during normal operation and allowing the at least one diode connected transistor to be selectively unbypassed during testing operations.

38. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

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coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling at least one bypass transistor to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

39. (New) The method of claim 38 wherein coupling at least one bypass transistor to a plurality of diode connected transistors includes coupling a plurality of bypass transistors to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

40. (New) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

41. (New) The method of claim 38 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.

42. (New) A method of forming an integrated circuit, comprising:

forming an array of memory cells on a substrate;

coupling a substrate voltage regulator circuit to the substrate for setting a substrate voltage bias level including:

coupling a series of diode connected transistors between a supply voltage source and the substrate; and

coupling a plurality of bypass transistors to a plurality of diode connected

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transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

43. (New) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally off bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors unbypassed during normal operation and allowing the plurality of diode connected transistors to be selectively bypassed during testing operations.

44. (New) The method of claim 42 wherein coupling a plurality of bypass transistors to a plurality of diode connected transistors includes coupling a plurality of normally on bypass transistors to a plurality of diode connected transistors leaving the plurality of diode connected transistors bypassed during normal operation and allowing the plurality of diode connected transistors to be selectively unbypassed during testing operations.